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10/598,584	09/05/2006	Adrianus Josephus Bink	NL04 0237 US1	7391

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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
09/30/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/598,584	BINK ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-9, 11, and 13-18 are pending.

2. The office acknowledges the following papers:

Specification, claims, arguments, drawings, and terminal disclaimer filed on 7/31/2009.

Withdrawn objections and rejections

3. The specification objections have been withdrawn due to amendment.

4. The drawing objections have been withdrawn.

5. The claim objections for claims 1-18 have been withdrawn due to amendment and cancellation of the claims.

6. The 35 U.S.C. §112 second paragraph rejections for claims 8, 10-12, and 18 are withdrawn due to amendment and cancellation of the claims.

Terminal Disclaimer

7. The terminal disclaimer filed on 7/31/2009 has not been approved due to the attorney signing it not being the attorney of record. An updated Power of Attorney form is required.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory

obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-18 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2 of copending Application No. 10/598,583 in view of Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878).

Instant Application	Application # 10/598,583
1. An electronic circuit comprising:	1. An electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:
First and second pipeline stages;	First and second pipeline stages, each of the first and second pipeline stages generating pipeline data;
A first latch positioned between the first and second pipeline stages; and	A latch positioned between the first and second pipeline stages; and
a first latch control circuit connected to the first latch, the latch control circuit receiving a first control signal, said first control signal being randomly-generated and indicating a mode of operation of the electronic circuit;	
Wherein the electronic circuit is adapted to operation in a normal mode in which the	Wherein the electronic circuit is controlled by a control signal based on a latency

first latch is opened and closed in response to an enable signal controlled by the first latch control circuit, and	period of each respective instruction of said plurality of types of instruction, said electronic circuit being controlled to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and
A reduced mode in which the first latch is held open by the first latch control circuit.	A reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the generated pipeline data to propagate, independent of the enable signal, through the latch; and
	Wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage.

Independent Claim 13 is similar to claim 1 and is rejected for the same reasons.

The limitations not shown by the claims in application # 10/598,583 are read upon as specified by the rejection below. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10. Claims 1-18 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 7,423,449 in view of Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878).

Instant Application	U.S. 7,423,449
1. An electronic circuit comprising:	1. An electronic circuit comprising:
First and second pipeline stages; and	First and second combinational logic blocks; and
A first latch positioned between the first and second pipeline stages; and	A latch positioned between the combinational logic blocks;
a first latch control circuit connected to the	

first latch, the latch control circuit receiving a first control signal, said first control signal being randomly-generated and indicating a mode of operation of the electronic circuit;	
Wherein the electronic circuit is adapted to operation in a normal mode in which the first latch is opened and closed in response to an enable signal controlled by the first latch control circuit, and	Wherein the electronic circuit is adapted to operation in a normal mode in which the latch is opened and closed in response to an enable signal, and
A reduced mode in which the first latch is held open by the first latch control circuit.	
	A test mode in which the latch is held open, such that the latch is transparent.

Independent Claim 13 is similar to claim 1 and is rejected for the same reasons. The limitations not shown by the claims in U.S. 7,423,449 are read upon as specified by the rejection below.

New Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1, 3-9, 11, and 13-18 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "said first control signal being randomly-generated" and "a reduced mode in which the first latch is held open by the first latch control circuit". The first claimed limitation seems to have written description support in at least paragraphs 33 and 46 of the PB-PUB. However, the limitations requires that the first control signal being randomly-generated causes a latch to be held open. Randomly holding the latch

open will cause data being processed to be lost, as disclosed in paragraph 46 of the PG-PUB. Paragraph 46 in fact states that the "signal generator is configured to operate such that the "random" signal is safe with regard to the latch operation." Thus, it seems that the signal being generated and sent to the first latch control circuit is conditional on safe operation. Thus, the signal isn't truly random at all, since the signal can't truly be randomly generated and sent to the first latch control signal. For examination purposes, the claimed limitation will be interpreted as generated the first control signal when a safe latching operation occurs.

Claims 9 and 13-14 recite similar limitations and are rejected for the same reasons.

13. Claims 3-8, 11, and 15-18 are rejected due to their dependency.

New Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1, 3-9, 11, and 13-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878).

16. As per claim 1:

Hennessy disclosed an electronic circuit comprising:

first and second pipeline stages (Hennessy: Figure 6.25, pipeline stages MEM and WB);

a first latch positioned between the first and second pipeline stages (Hennessy: Figure 6.25, MEM/WB pipeline register)(It's obvious to one of ordinary skill in the art that the pipeline register can be implemented as a latch.); and

wherein the electronic circuit is adapted to operate in a normal mode in which the first latch is opened and closed in response to an enable signal controlled by the first latch control circuit (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal.).

Hennessy failed to teach a first latch control circuit connected to the first latch, the latch control circuit receiving a first control signal, said first control signal being randomly-generated and indicating a mode of operation of the electronic circuit and a reduced mode in which the latch is held open by the first latch control circuit.

However, Colwell disclosed a first latch control circuit connected to the first latch, the latch control circuit receiving a first control signal (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The recent KSR ruling supports that a claim would have been obvious because "a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely that the product is not of innovation but of ordinary skill and common sense." One of ordinary skill in the art would look at the Hennessy reference and realize that there are a finite

number of ways for an ALU type instruction to bypass the MEM/WB pipeline register to allow for early retirement in the fourth clock cycle of the instruction. One of these ways would be to allow the MEM/WB pipeline register to be kept open during the fourth clock cycle of the ALU type instruction, which allows for the ALU result to flow out of the MEM/WB pipeline register, through the MUX, and be written into the register file during the fourth clock cycle. Thus, it would have been obvious to one of ordinary skill in the art to choose one of the finite number of solutions, i.e. keep the MEM/WB pipeline register open, to allow for the bypassing teachings of Colwell to be implemented in Hennessy. The control logic output is the first control signal that overrides the clock signal to keep the pipeline register open and the control circuit is the logic that implements the override.), said first control signal being randomly-generated and indicating a mode of operation of the electronic circuit (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(In view of the 112 rejection, the limitation is interpreted as the control signal being generated when a safe latching operation can occur. It's obvious to one of ordinary skill in the art that the control logic of Colwell only sends out a control signal when a safe bypassing operation can occur. Thus, reading on the limitation. The signal indicates a reduced mode that holds open the pipeline register of Hennessy.).

a reduced mode in which the latch is held open by the first latch control circuit (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(As stated above, in view of the recent KSR ruling, it would have been obvious to one of ordinary skill in the art to choose one of the

finite number of solutions, i.e. keep the MEM/WB pipeline register open, to allow for the bypassing teachings of Colwell to be implemented in Hennessy. The reduced mode is the mode where the control logic of Colwell overrides the clock signal of Hennessy.).

The advantage of bypassing an extra pipeline stage that isn't needed for instructions is that these instructions will be allowed to retire earlier and result in increased performance when there is no writeback contention (Colwell: Column 2 lines 65-67 continued to column 3 lines 1-9). One of ordinary skill in the art would have been motivated to modify Hennessy to perform the pipeline stage bypassing of Colwell for the advantage above. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the pipeline stage bypassing of Colwell into the processor of Hennessy for the advantage of increasing performance of the processor of Hennessy.

17. As per claim 3:

Hennessy and Colwell disclosed the electronic circuit of claim 1, the electronic circuit further comprising a third pipeline stage and a second latch, the second latch positioned between the second and third pipeline stages (Hennessy: Figure 6.25, pipeline stages EX and MEM)(The third pipeline stage can be considered the execution stage, where the latch is the EX and MEM pipeline stages.).

18. As per claim 4:

Hennessy and Colwell disclosed the electronic circuit of claim 3, wherein, when the electronic circuit is operating in the reduced mode, the first and second latches are held open (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column

8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The advantage of longer pipelines is that increased performance can be achieved by executing more instructions in parallel. Official notice is given that pipelines can be of greater length than five stages. Thus, it's obvious to one of ordinary skill in the art that pipelines can be longer than five stages. With a longer pipeline, the data memory and writeback stages can be multiple stages, which requires multiple latches to be opened to execute instructions that don't use the data memory stage.).

19. As per claim 5:

Hennessy and Colwell disclosed the electronic circuit of claim 3, wherein, when the electronic circuit is operating in the reduced mode, one of the first and the second latches is held open (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(As stated above in claim 1, in view of the recent KSR ruling, it would have been obvious to one of ordinary skill in the art to choose one of the finite number of solutions, i.e. keep the MEM/WB pipeline register open, to allow for the bypassing teachings of Colwell to be implemented in Hennessy. The first latch is held open during the reduced mode.).

20. As per claim 6:

Hennessy and Colwell disclosed the electronic circuit of claim 5, wherein the one of the first and second latches held open changes over time (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(As stated above in claim 1, in view of the recent KSR ruling, it would have been obvious to one of ordinary skill in the art to choose one of the finite number

of solutions, i.e. keep the MEM/WB pipeline register open, to allow for the bypassing teachings of Colwell to be implemented in Hennessy. Both latches are held open in normal mode when clocked, and a single latch is held open in reduced mode to allow an ALU type instruction to bypass the MEM stage. Thus, the latches held open changes during executing a program.).

21. As per claim 7:

Hennessy and Colwell disclosed the electronic circuit of claim 6, wherein the first and second latches are held open for different lengths of time (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(As stated above in claim 1, in view of the recent KSR ruling, it would have been obvious to one of ordinary skill in the art to choose one of the finite number of solutions, i.e. keep the MEM/WB pipeline register open, to allow for the bypassing teachings of Colwell to be implemented in Hennessy. The first latch is the latch between the MEM and WB stages and the second latch is the latch between the EX and MEM stages. The first latch can be held open by the control signal outputted from the control logic of Colwell. Thus, the first latch can be held open for a different amount of time than the second latch.).

22. As per claim 8:

Hennessy and Colwell disclosed the electronic circuit of claim 1, wherein the electronic circuit operates in the reduced mode for varying time periods (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(As stated above in claim 1, in view of the recent KSR

ruling, it would have been obvious to one of ordinary skill in the art to choose one of the finite number of solutions, i.e. keep the MEM/WB pipeline register open, to allow for the bypassing teachings of Colwell to be implemented in Hennessy. The MEM/WB pipeline register can operate in reduced mode for different lengths of time dependent upon the type of instructions sent into the pipeline.).

23. As per claim 9:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 3, further comprising a second latch control circuit connected to the second latch, said second latch control circuit receiving a second control signal (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The advantage of longer pipelines is that increased performance can be achieved by executing more instructions in parallel. Official notice is given that pipelines can be of greater length than five stages. Thus, it's obvious to one of ordinary skill in the art that pipelines can be longer than five stages. With a longer pipeline, the data memory and writeback stages can be multiple stages, which requires multiple latches to be opened to execute instructions that don't use the data memory stage. Therefore, multiple pipeline registers, instead of just the MEM/WB pipeline register as stated in claim 1, would receive control signals to override the clock signal.), said second control signal being randomly-generated and indicating the mode of operation of the electronic circuit (Hennessy: Figures 6.32 and 6.33, load instruction)(The EX/MEM pipeline register is opened and closed by the inherent clock signal of the processor not shown, which controls the second latch.), said second control signal being randomly-

generated and indicating the mode of operation of the electronic circuit (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(In view of the 112 rejection, the limitation is interpreted as the control signal being generated when a safe latching operation can occur. It's obvious to one of ordinary skill in the art that the control logic of Colwell only sends out a control signal when a safe bypassing operation can occur. Thus, reading on the limitation. The signal indicates a reduced mode that holds open the pipeline register of Hennessy.).

24. As per claim 11:

Hennessy and Colwell disclosed the electronic circuit of claim 9, wherein the first and second signals indicate whether the first latch, the second latch or both latches are to be held open when the electronic circuit is operating in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The multiple pipeline registers, instead of just the MEM/WB pipeline register as stated in claim 9, would receive control signals to override the clock signal. These signals determine if the multiple pipeline registers are held open or operate normally.).

25. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Therefore, claim 13 is rejected for the same reasons as claim 1.

26. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 9. Therefore, claim 14 is rejected for the same reason(s) as claim 9.

27. As per claim 15:

Hennessy and Colwell disclosed the method of claim 14, wherein the first latch and the second latch are held open at different times when the electronic circuit is operating in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(As noted in claim 9, the pipeline can have a plurality of execution or memory write-back pipeline stages. These stages read on the first and second latches. It's obvious to one of ordinary skill in the art that if these stages are held open by the control logic as described by Colwell, then the first stages will be the first to be closed when a bypass operation can't be performed.).

28. As per claim 16:

The additional limitation(s) of claim 16 basically recite the additional limitation(s) of claim 7. Therefore, claim 16 is rejected for the same reason(s) as claim 7.

29. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 4. Therefore, claim 17 is rejected for the same reason(s) as claim 4.

30. As per claim 18:

The additional limitation(s) of claim 18 basically recite the additional limitation(s) of claim 8. Therefore, claim 18 is rejected for the same reason(s) as claim 8.

Response to Arguments

31. The arguments presented by Applicant in the response, received on 7/31/2009 are partially considered persuasive.

32. Applicant argues "Hennessy in view of Colwell fails to teach, disclose, or suggest, "a first latch control circuit connected to the first latch, said latch control circuit to receive a first control signal, said first control signal being randomly-generated and indicating the mode of operation of the electronic circuit," as recited in claim 1 and similarly recited in claim 13. As discussed above, the claimed latch control circuit receives an independent signal that is randomly-generated for the purpose of hiding current peaks in the associated latches. This varies significantly from the combination of Hennessy and Colwell, which fails to disclose an independent, randomly-generated signal to control when a latch is held open."

This argument is partially found to be persuasive for the following reason. The examiner agrees that the combination of Hennessy and Colwell failed to teach randomly allowing for pipeline registers to be held open according to generated control signals. The combination instead allows for a pipeline register to be held open if the control logic of Colwell detects that a bypassing operation can occur (i.e. an instruction can retire a pipeline stage early.). However, as noted in the 112 2nd paragraph rejection above, the newly claimed limitation would cause the processor to randomly hold a latch open that will cause data being processed to be lost. Paragraph 46 in fact states that the "signal generator is configured to operate such that the "random" signal is safe with regard to the latch operation." Thus, it seems that the signal being generated and sent to the first

latch control circuit is conditional on safe operation. Thus, the signal isn't truly random at all, since the signal can't truly be randomly generated and sent to the first latch control signal. Therefore, the newly added limitations are interpreted for examination purposes as generating the first control signal when a safe latching operation occurs.

This interpretation is disclosed by the combination of Hennessy and Colwell. The combination, as noted above, allows for the MEM/WB pipeline register to be held open when a safe bypassing operation can occur, as determined by the control logic element 62 of Colwell. Thus, the combination reads upon the newly cited limitations in view of the 112 2nd paragraph rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
Examiner, Art Unit 2183